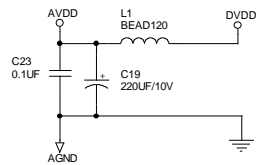
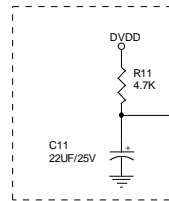


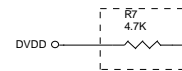
Note: DVDD is 3.3V.



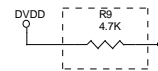
Note5: R11,C11 is for power on reset. It can also be reset by Host Processor.



Note1: 16/32 bit selection; Removed R7 when using 16-bit mode; otherwise is 32-bit mode.



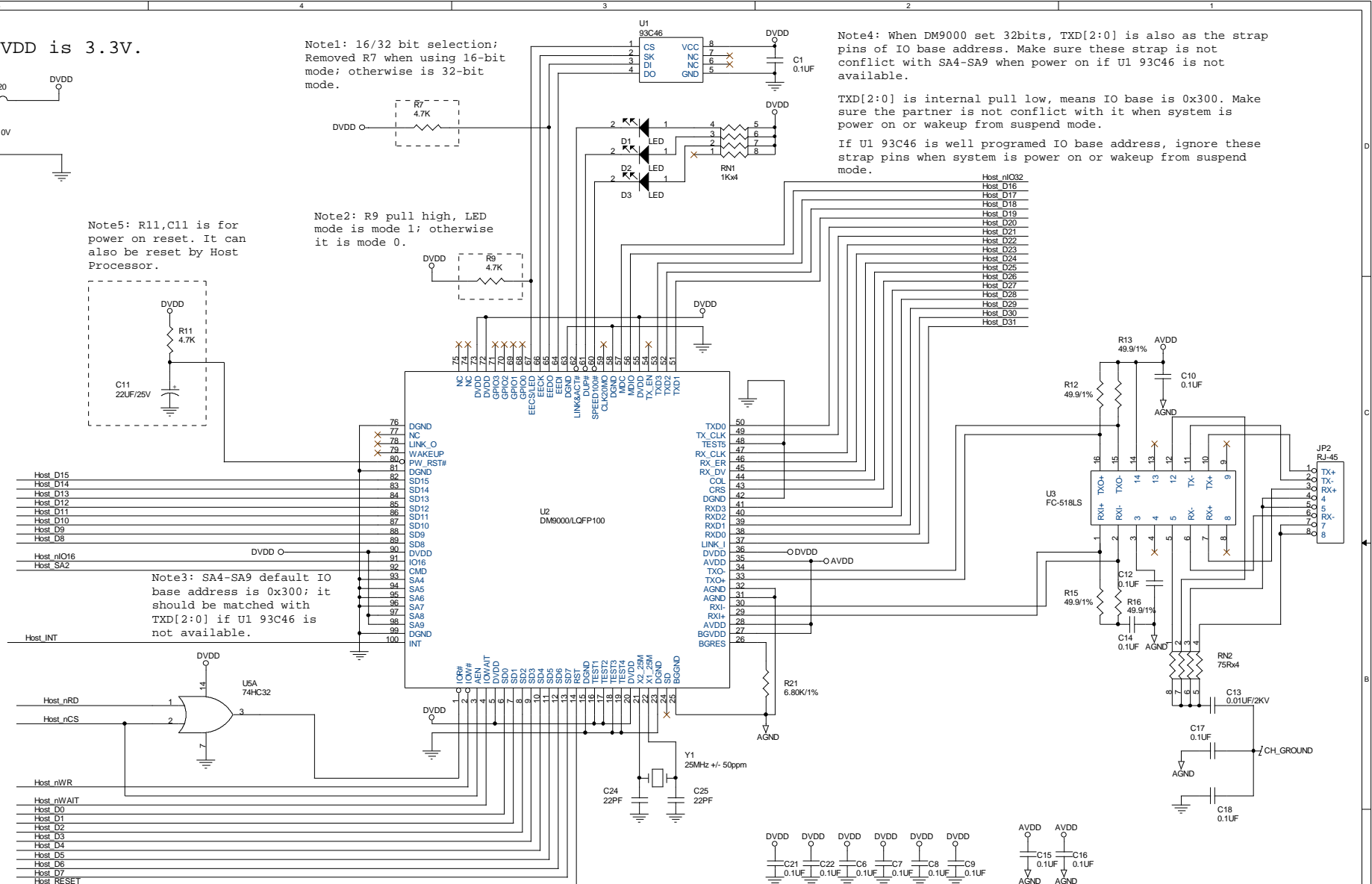
Note2: R9 pull high, LED mode is mode 1; otherwise it is mode 0.



Note4: When DM9000 set 32bits, TXD[2:0] is also as the strap pins of IO base address. Make sure these strap is not conflict with SA4-SA9 when power on if U1 93C46 is not available.

TXD[2:0] is internal pull low, means IO base is 0x300. Make sure the partner is not conflict with it when system is power on or wakeup from suspend mode.

If U1 93C46 is well programed IO base address, ignore these strap pins when system is power on or wakeup from suspend mode.



IO base address = Host_nCS

IO data address = Host_nCS + 0x04 (if Host_SA2 connect to CMD (92pin))

**Note: DM9000 Host Parallel Bus, for 16/32bits
For Application Reference Design Only**

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Size		
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Rev		
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